REMARKS

Claims 1-3, 5 have been rejected under 35 USC 102(e) as being anticipated by U.S. patent no. 6,222,269 ("Usami").

Claims 1-2, 13-14, 21-23 have been rejected under 35 USC 102(b) as being anticipated by U.S. patent no. 5,045,870 ("Lamey").

Claims 1, 6-13, 15, 17-20, 22, 24, 26-30 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 6,365,529 ("Hussein") in view of Lamey.

Claims 4, 16 and 25 have been designated as having allowable subject matter by being objected to as being dependent upon a rejected base claim. Applicants have incorporated one of the elements from each of claims 4, 16, 25 into the corresponding independent claims 1, 13, 22. Applicants maintain that claims 1, 13 and 22 are now allowable over the cited prior art because these claims contain the allowable subject matter that was previously deemed allowable by the Examiner. Claims 3-12, 15-21, 23-30 depend from claims 1, 13 and 22, respectively, and therefore are also allowable over the cited prior art. Claims 2 and 14 have been cancelled as redundant.

CONCLUSION

Applicants submit that claims 1, 3-13 and 15-30 are now in condition for allowance, and indication of allowance is respectfully requested. If fees or credits are found that are not otherwise covered, please charge or credit Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

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John Travis
Reg. No. 43,203

12400 Wilshire Blvd, Seventh Floor
Los Angeles, California 90025-1026
(512) 330-0844

APPENDIX A

Marked-up version of amended claims:

1. (Amended twice) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a first barrier layer on the surface of the first patterned conductive layer;

forming a second barrier layer on the surface of the first barrier layer;

forming a dielectric layer on the surface of the second barrier layer; and

forming one of a via and a trench through a first portion of the dielectric layer and through a first portion of one of the first and second barrier layers;

wherein the via is filled with a sacrificial light absorbing material.

2. (Cancelled)

3. (Amended once) The method of claim [2] 1 further comprising forming [a] the trench through a second portion of the dielectric layer if the via is formed through the first portion of the dielectric layer.

4. (Amended once) The method of claim [3] 1, wherein the [via is filled with a] sacrificial light absorbing material [comprising] comprises at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer.

5. (Amended once) The method of claim [2] 1 further comprising forming [a] the via through a second portion of the dielectric layer if the trench is formed through the first portion of the dielectric layer.

6. (Amended once) The method of claim [3] 1 further comprising forming said one of the via and the trench through the second barrier layer followed by forming said one of the via and the trench through the first barrier layer.

7. (Amended once) The method of claim 6 wherein said one of the via and the trench is formed through the first and the second barrier layer with a single etch pass.

13. (Amended twice) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a first barrier layer comprising silicon nitride on the surface of the first patterned conductive layer;

forming a second barrier layer comprising silicon carbide on the surface of the first barrier layer; [and]

forming a dielectric layer on the surface of the second barrier layer; and

forming, through a first portion of the dielectric layer, either of a via and a trench filled with a sacrificial light absorbing material;

14. (Cancelled)

15. (Amended once) The method of claim [14] 13 further comprising forming [a] the trench through a second portion of the dielectric layer if the via is formed through the first portion of the dielectric layer.

16. (Amended once) The method of claim [15] 13, wherein the [via is filled with a] sacrificial light absorbing material [comprising] comprises at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer.

17. (Amended once) The method of claim [15] 13 further comprising forming [a] the via through a second portion of the dielectric layer if the trench is formed through the first portion of the dielectric layer.

18. (Amended once) The method of claim [14] 13 wherein said either of the via and the trench is formed through the first and the second barrier layer with a single etch pass.

19. (Amended once) The method of claim 13 wherein the first barrier layer [comprising silicon nitride] comprises between 1 nanometer and 7 nanometer of silicon nitride.

20. (Amended once) The method of claim 13 wherein the second barrier layer [comprising silicon carbide] comprises less than 200 nanometers of silicon carbide.

21. (Amended once) The method of claim 13 wherein at least one of the silicon nitride and the silicon carbide is deposited using any one of a plasma enhanced chemical vapor deposition process, a chemical vapor deposition process and an atomic layer deposition process.

22. (Amended twice) A method of forming a semiconductor device comprising:

forming a first patterned conductive layer on a dielectric material on a substrate;

forming a first barrier layer comprising silicon nitride on the surface of the first patterned conductive layer;

forming a second barrier layer on the surface of the first barrier layer;

forming a dielectric layer on the surface of the second barrier layer; and

forming a via filled with sacrificial light absorbing material through a first portion of the dielectric layer and through a first portion of one of the first and second barrier layers.

25. (Amended once) The method of claim 24, wherein the [via is filled with a] sacrificial light absorbing material [comprising] comprises at least one of a dyed spin-on polymer and a dyed spin-on glass with dry etch properties similar to the dielectric layer.